DEPARTMENT OF APPLIED ELECTRONICS & INSTRUMENTATION ENGINEERING
C.V.RAMAN COLLEGE OF ENGINEERING

Training Modules (Session-2012-16)

Semesters	Hours	Compulsory course-I	Compulsory Course-II
3rd	45	LabVIEW-1(45 hrs.)	
4th	45	LabVIEW-2(25 hrs.)	Digital VLSI Design (20 hrs.)
5th	65	LabVIEW-3(30 hrs.)	Analog VLSI Design (35 hrs.)
7th	65	LabVIEW-4(30 hrs.)	Mixed VLSI Design (35 hrs.)

LABVIEW CENTRE OF EXCELLENCE

COURSE: LabVIEW Core – 1

DURATION: 45 Hours

OBJECTIVE

- Understand front panels, block diagrams, icons, and connector panes
- Create user interfaces with charts, graphs and buttons
- Use the programming structures and data types that exist in LabVIEW
- Use various editing and debugging techniques
- Create and save VIs for use as subVIs
- Display and log data
- Create applications that use data acquisition (DAQ) devices
- Create applications that use GPIB and serial port instruments
- Use the state machine design pattern in your applications
- Use local variables to modify front panel controls or stop parallel loops

TRAINING METHODOLOGY

Explanation, Demonstration and hands-on practice.

COURSE CONTENTS

- Navigating LabVIEW
- Troubleshooting and Debugging Vis
- Implementing a VI
- Developing Modular Applications
- Creating and Leveraging Data Structures
- Managing File and Hardware Resources

- Using Sequential and State Machine Algorithms
- Solving Dataflow Challenges with Variables

COURSE: LabVIEW Core– 2

DURATION: 25 Hours

PREREQUISITES
knowledge of LabVIEW Core – 1

OBJECTIVE

- Apply common design patterns that use queues and events
- Use event programming effectively
- Programmatically control user interface objects
- Evaluate file I/O formats and use them in applications
- Modify existing code for improved usability
- Prepare, build, debug, and deploy stand-alone applications

TRAINING METHODOLOGY

Explanation, Demonstration and hands-on practice.

COURSE CONTENTS

- Moving Beyond Dataflow
- Implementing Design Patterns
- Controlling the User Interface
- File I/O Techniques
- Improving an existing VI
- Deploying an application

COURSE: LabVIEW– 3

DURATION: 30 Hours

PREREQUISITES

Knowledge of LabVIEW Core – 1

OBJECTIVE

- Design to enabled educators to easily teach microcontroller programming concepts
- Learn graphical programming, in conjunction with traditional embedded system concepts like interrupts handling, on-chip I/O and software optimization
- To design, implement, document, and test LabVIEW applications
- To reduce development time and improve application stability.

TRAINING METHODOLOGY

Explanation, Demonstration and hands-on practice.

COURSE CONTENTS

- Introduction to LabVIEW Embedded Module for ARM Microcontrollers.
- Getting Started with Cortex – M3
- Programming Using Cortex – M3
- Getting Started with ARM 7
- Programming Using ARM7
- Introduction to NI ELVIS – II Kit.
- Getting Started with NI ELVIS – II
- Programming Using NI ELVIS – II

COURSE: LabVIEW– 4

DURATION: 30 Hours

PREREQUISITES

Knowledge of LabVIEW Core – 1

OBJECTIVE

- Create & compile your LabVIEW FPGA
- Acquire and generate analog and digital signals, control timing, synchronize operations, and implement signal processing on the FPGA
- Communicate between the FPGA and a host
- Design and implement applications using the LabVIEW FPGA module

TRAINING METHODOLOGY

Explanation, Demonstration and hands-on practice.

COURSE CONTENTS

- Introduction to LabVIEW FPGA
- Getting Started with LabVIEW FPGA
- Programming Using LabVIEW FPGA
- Using FPGA I/O
- Timing an FPGA VI
- Executing Code in Single-Cycle Timed Loops

VLSI CENTRE OF EXCELLENCE

TRAINING MODULES

COURSE: DIGITAL VLSI DESIGN (25 hours)

SEMESTER -4th

COURSE COVERAGE – Focus areas

This course will enhance the knowledge of the students in the most important aspects of VLSI Technology. The course has been structured keeping in view the current development in the field of VLSI Design and its effect on the society. The development of the course tries to address the gap between academia course curriculum and semiconductor industry expectations.

The key modules of the framework are

- Concepts of Digital Design using Verilog
- FPGA Architectures & Design Flow
- ASIC Design

COURSE OBJECTIVE

This course will enable the students to

- Identify the various steps in VLSI Design flow
- Understand and Differentiate between ASIC & FPGA Design flow
- Understand the difference in VLSI design styles: FPGA, Standard Cell Design & Full Custom Design
- Understand the basic concepts and programming styles of Verilog HDL
- Apply the concepts of Digital System Design to model a digital logic block for the given specifications
- Design a synthesizable RTL solution with all the design rules & optimization methodologies.
- Implement the synthesized design blocks on a target Xilinx Device and optimize the design for the given specifications.

PRE-REQUISITES: The students should have a basic knowledge of

- Digital Electronics Circuits
- Basics of Electronics

TRAINING MODULES

Sl. No.	Topic
1	Introduction to Digital Electronics Circuits
2	ASIC Design Flow for Digital Designs, FPGA Design Flow
3	Basic Concepts of Verilog HDL
4	Defining Module and Ports in Verilog HDL, Tasks & Functions
5	Behavioral, Structural and Dataflow Coding Styles of digital circuits
6	Testbench creation using Verilog HDL

7	FPGA Design using Xilinx, Concept of CLBs, Switch Matrix
8	Standard Cell Based Design, Full Custom Design
9	RTL Synthesis
10	Introduction to Xilinx ISE Tool
11	HDL Coding of Simple logic gates using Xilinx ISE
12	HDL Coding of half adder (HA) and full adder (FA) using Xilinx ISE
13	HDL Coding of half subtractor (HS) and full subtractor (FS) using Xilinx ISE
14	HDL Coding of decoders and encoders using Xilinx ISE
15	HDL Coding of multiplexers and de-multiplexers using Xilinx ISE
16	HDL Coding of latches using Xilinx ISE
17	HDL Coding of flipflops using Xilinx ISE
18	HDL Coding of Simple logic gates using HDL Designer
19	HDL Coding of HA, HS, FA & FS using HDL Designer
20	HDL Coding of decoders and encoders using HDL Designer
21	HDL Coding of multiplexers and de-multiplexers using HDL Designer
22	HDL Coding of latches using HDL Designer
23	HDL Coding of flipflops using HDL Designer
24	Functional Verification using Modelsim
25	RTL Synthesis, Floorplanning, Placement, Routing of Digital circuits using Xilinx ISE
26	RTL Synthesis, Floorplanning, Placement, Routing of Digital circuits using Xilinx ISE
27	Design optimization for given design specifications
28	Post Synthesis simulation using Precision RTL
29	Power and Timing Analysis & Optimization for a given Xilinx design
30	Programming target device using IMPACT

COURSE:ANALOG VLSI DESIGN (30HOURS)
SEMESTER: 5th
COURSE COVERAGE – Focus areas
This course will enhance the knowledge of the students in the most important aspects of Analog VLSI Design. The course has been structured keeping in view the current development in the field of Analog VLSI Design and its effect on the society. The development of the course tries to keep the student abreast with the changes in the semiconductor industry.

The key modules of the framework are

- Concepts of Analog VLSI Design using SPICE
- Design of Amplifiers using BJTs and MOSFETs
- Analog Design Flow

COURSE OBJECTIVE
This course will enable the students to

- Identify the various steps in Analog Design flow
- Understand and Differentiate between Digital & Analog Design flow
- Understand the concepts of MOSFETs and CMOS Design
- Design the schematic of any logic gate using CMOS circuits
- Analyze the performance and characteristics of the designed CMOS circuits
- Understand the underlying concepts of an amplifier design
- Perform the simulation and synthesis of analog circuits using Mentor Graphics tools.

PRE-REQUISITES:
The students should have a basic knowledge of

- Digital Electronics Circuits
- Analog Electronics Circuits
- Basics of Electronics

TRAINING MODULES

Sl. No.	Topic
1	Analogue Design Flow
2	Basics of Analog CMOS Design
3	BJT Amplifier Circuit: Input and Output Characteristics
4	MOSFET Amplifier Circuit: Transfer & Drain Characteristics
5	CMOS Fabrication Technology
6	Introduction to SPICE, Coding Styles Using SPICE
7	Analogue Circuit Simulation: Verification using SPICE Codes

8	Concepts of Differential Amplifiers
9	Concepts of Current Mirrors
10	Concept of Stick Diagrams, Layout and Design Rules
11	DRC, LVS of Analogue Circuits
12	SPICE Synthesis and Extraction of Netlist
13	RC Extraction, Post-RC STA of Analogue circuits & Back Annotation
14	Introduction to Mentor Graphics Analog Tool Bundle
15	Introduction to setting up environment variables
16	Introduction to initiation of different tools in Linux Environment
17	Introduction to setting up work directories for different tools
18	Schematic Design of Analogue Circuits with Design Architect
19	BJT Amplifier Circuit Simulation: CB & CE Configuration
20	MOSFET Amplifier Circuit Simulation: CS & CG Configuration
21	Schematic Simulation using Eldo
22	Design and Simulation of CMOS Inverter with Design Architect
23	Layout Design using IC station for the given CMOS Inverter
24	Physical Verification using Calibre for the given CMOS Inverter
25	Design and Simulation of CMOS NAND gate with Design Architect
26	Layout Design using IC station for the given CMOS NAND gate
27	Physical Verification using Calibre for the given CMOS NAND gate
28	Design and Simulation of CMOS NAND gate with Design Architect
29	Layout Design using IC station for the given CMOS NOR gate

30	Physical Verification using Calibre for the given CMOS NOR gate
31	Design and Simulation of CMOS AND gate with Design Architect
32	Layout Design using IC station for the given CMOS AND gate
33	Physical Verification using Calibre for the given CMOS AND gate
34	Design and Simulation of CMOS OR gate with Design Architect
35	Layout Design using IC station for the given CMOS OR gate
36	Physical Verification using Calibre for the given CMOS OR gate
37	Design and Simulation of Differential Amplifiers
38	Design and Simulation of Current Mirrors with given specifications
39	Design and Simulation of DACs with given specifications
40	Layout Design using IC station for the given SPICE netlist

COURSE:VLSI Design(35hrs)

SEMESTER: 7th

COURSE COVERAGE – Focus areas

This course will enhance the knowledge of the students in the most important aspects of VLSI Design. The course has been structured keeping in view the current development in the field of VLSI Design and its effect on the society. The development of the course tries to keep the student abreast with the changes in the semiconductor industry.

The key modules of the framework are

- Concepts of Digital Design using Verilog
- FPGA Architectures & Design Flow
- Concepts of Analog VLSI Design using SPICE
- Analog Design Flow

COURSE OBJECTIVE

This course will enable the students to

- Identify the various steps in VLSI Design flow
- Understand and Differentiate between ASIC & FPGA Design flow
- Understand the basic concepts and programming styles of Verilog HDL
- Implement a given digital system as an ASIC using Mentor Graphics front end

and back end tools.

- Identify the various steps in Analog Design flow
- Understand and Differentiate between Digital & Analog Design flow
- Understand the concepts of MOSFETs and CMOS Design
- Design the schematic of any logic gate using CMOS circuits

PRE-REQUISITES:

The students should have a basic knowledge of

- Digital Electronics Circuits
- Analog Electronics Circuits
- Basics of Electronics

TRAINING MODULES

Sl. No.	Topic
1	Mixed–Signal Design Flow
2	Review of Digital Circuit Design
3	Review of Analogue Circuit Design
4	Design and simulation of a digital circuit using HDL Designer
5	RTL synthesis of the digital circuit using Leonardo Spectrum
6	Design & Simulation of an analog circuit using Design Architect
7	Extracting the SPICE code of a digital circuit
8	Extracting the SPICE code of an analog circuit
9	Combining the SPICE of analog and digital circuit
10	Floor planning& Placement of the mixed-signal circuit
11	Routing the net list of the mixed-signal circuit
12	RC Extraction, Post-RC STA of the mixed-signal circuit
13	Concept of DACs and ADCs
14	Design Libraries

15	Static Timing Analysis & Back Annotation
16	Concepts of DFT (BIST, ATPG, Scan Insertions)
17	DFT assertions, Pre & Post DFT Checks
18	Schematic Design using Design Architect
19	Schematic Simulation using Eldo
20	Design & Simulation of Mixed Mode design block using Eldo&Modelsim
21	Project Work

For feedback and suggestion please write to trainingfeedback@cvrgi.edu.in