DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING
C.V.RAMAN COLLEGE OF ENGINEERING

Training Modules (Session-2012-16)

SEMESTER	HOURS	COMPULSORY-I	COMPULSORY-II
3rd	45	VLSI Design (25 Hours)	Industrial Automation-I for ETC (20 Hours)
4th	45	VLSI Design (25 Hours)	Industrial Automation-I for ETC (20 Hours)
5th	65	VLSI Design (30 Hours)	Industrial Automation-II for ETC (35 Hours)
7th	65	VLSI Design (30 Hours)	Industrial Automation-III for ETC (35 Hours)

DIGITAL VLSI DESIGN(25 hours)

SEMESTER -3rd &4th

COURSE COVERAGE – Focus areas

This course will enhance the knowledge of the students in the most important aspects of VLSI Technology. The course has been structured keeping in view the current development in the field of VLSI Design and its effect on the society. The development of the course tries to address the gap between academia course curriculum and semiconductor industry expectations.

The key modules of the framework are

- Concepts of Digital Design using Verilog
- FPGA Architectures & Design Flow
- ASIC Design

COURSE OBJECTIVE

This course will enable the students to

- Identify the various steps in VLSI Design flow
- Understand and Differentiate between ASIC & FPGA Design flow
- Understand the difference in VLSI design styles: FPGA, Standard Cell Design & Full Custom Design
- Understand the basic concepts and programming styles of Verilog HDL
- Apply the concepts of Digital System Design to model a digital logic block for the given specifications
- Design a synthesizable RTL solution with all the design rules & optimization methodologies.
- Implement the synthesized design blocks on a target Xilinx Device and optimize the design for the given specifications.

PRE-REQUISITES: The students should have a basic knowledge of

- Digital Electronics Circuits
- Basics of Electronics

TRAINING MODULES

Sl. No.	Topic
1	Introduction to Digital Electronics Circuits (Combinational Circuits)
2	FPGA Design Flow
3	Full-custom & Semicustom IC Flow
4	Basic Concepts of Verilog HDL
5	Defining Module and Ports in Verilog HDL, Tasks & Functions
6	Structural and Dataflow Coding Styles of various combinational circuits
7	Functional Verification using Verilog HDL Testbench
8	FPGA Design using Xilinx, Concept of CLBs, Switch Matrix, IOBs
9	Introduction to Xilinx ISE Tool
10	HDL Coding of Simple logic gates using Xilinx ISE
11	HDL Coding of half adder and full adder using Xilinx ISE
12	HDL Coding of half subtractor and full subtractor using Xilinx ISE
13	HDL Coding of decoders and encoders using Xilinx ISE
14	HDL Coding of multiplexers and demultiplexers using Xilinx ISE
15	HDL Coding of code converters and multiplier using Xilinx ISE
16	HDL Coding of logic unit using Xilinx ISE
17	HDL Coding of Simple logic gates using HDL Designer
18	HDL Coding of half adder and full adder using HDL Designer
19	HDL Coding of half subtractor and full subtractor using HDL Designer
20	HDL Coding of decoders and encoders using HDL Designer

21	HDL Coding of multiplexers and demultiplexers using HDL Designer
22	HDL Coding of code converters and multiplier using HDL Designer
23	HDL Coding of logic unit using HDL Designer
24	Design entry of combo circuit from Truth Table using HDL Designer
25	Design entry of combo circuit from Truth Table using HDL Designer
26	Design entry of digital circuit from Block Diagram using HDL Designer
27	Design entry of digital circuit from Block Diagram using HDL Designer
28	Functional Verification using Modelsim/Questasim
29	RTL Synthesis, Floorplanning, Placement using Xilinx ISE
30	Routing of Digital circuits using Xilinx ISE

VLSI DESIGN (25 hours)

Sl. No.	Topic
1	Introduction to Digital Electronics Circuits (Sequential Circuits)
2	ASIC Design Flow for Digital Designs
3	Netlist to GDSII Design Flow
4	Basic Concepts of Verilog HDL
5	Defining Module and Ports in Verilog HDL, Tasks & Functions
6	Behavioral and Structural Coding Styles of various sequential circuits
7	Functional Verification using Verilog HDL Testbench
8	Standard Cell Based Design, Full Custom Design
9	RTL Synthesis

10	HDL Coding of latches and flipflops using Xilinx ISE
11	HDL Coding of latches and flipflops using Xilinx ISE
12	HDL Coding of shift registers using Xilinx ISE
13	HDL Coding of binary counters using Xilinx ISE
14	HDL Coding of binary counters using Xilinx ISE
15	HDL Coding of latches and flipflops using HDL Designer
16	HDL Coding of latches and flipflops using HDL Designer
17	HDL Coding of shift registers using HDL Designer
18	HDL Coding of binary counters using HDL Designer
19	HDL Coding of binary counters using HDL Designer
20	Design entry of digital circuit from Block Diagram using HDL Designer
21	Design entry of digital circuit from State Diagram using HDL Designer
22	Functional Verification using Modelsim/Questasim
23	RTL Synthesis, Floorplanning, Placement, Routing of Digital circuits using Xilinx ISE
24	RTL Synthesis of Digital circuits using Leonardo Spectrum
25	Design optimization for given design specifications
26	Post Synthesis simulation using Precision RTL
27	Power and Timing Analysis & Optimization for a given Xilinx design
28	Programming target device using IMPACT
29	Floorplanning and Placement using Mentor Calibre
30	Routing & RC Extraction using Mentor Calibre

ANALOG VLSI DESIGN (30HOURS)

SEMESTER: 5th

COURSE COVERAGE – Focus areas

This course will enhance the knowledge of the students in the most important aspects of Analog VLSI Design. The course has been structured keeping in view the current development in the field of Analog VLSI Design and its effect on the society. The development of the course tries to keep the student abreast with the changes in the semiconductor industry.

The key modules of the framework are

- Concepts of Analog VLSI Design using SPICE
- Design of Amplifiers using BJTs and MOSFETs
- Analog Design Flow

COURSE OBJECTIVE

This course will enable the students to

- Identify the various steps in Analog Design flow
- Understand and Differentiate between Digital & Analog Design flow
- Understand the concepts of MOSFETs and CMOS Design
- Design the schematic of any logic gate using CMOS circuits
- Analyze the performance and characteristics of the designed CMOS circuits
- Understand the underlying concepts of an amplifier design
- Perform the simulation and synthesis of analog circuits using Mentor Graphics tools.

PRE-REQUISITES:

The students should have a basic knowledge of

- Digital Electronics Circuits
- Analog Electronics Circuits
- Basics of Electronics

TRAINING MODULES

Sl. No.	Topic
1	Analogue Design Flow
2	Basics of Analog CMOS Design
3	BJT Amplifier Circuit: Input and Output Characteristics
4	MOSFET Amplifier Circuit: Transfer & Drain Characteristics
5	CMOS Fabrication Technology
6	Introduction to SPICE, Coding Styles Using SPICE
7	Analogue Circuit Simulation: Verification using SPICE Codes

8	Concepts of Differential Amplifiers
9	Concepts of Current Mirrors
10	Concept of Stick Diagrams, Layout and Design Rules
11	DRC, LVS of Analogue Circuits
12	SPICE Synthesis and Extraction of Netlist
13	RC Extraction, Post-RC STA of Analogue circuits & Back Annotation
14	Introduction to Mentor Graphics Analog Tool Bundle
15	Introduction to setting up environment variables
16	Introduction to initiation of different tools in Linux Environment
17	Introduction to setting up work directories for different tools
18	Schematic Design of Analogue Circuits with Design Architect
19	BJT Amplifier Circuit Simulation: CB & CE Configuration
20	MOSFET Amplifier Circuit Simulation: CS & CG Configuration
21	Schematic Simulation using Eldo
22	Design and Simulation of CMOS Inverter with Design Architect
23	Layout Design using IC station for the given CMOS Inverter
24	Physical Verification using Calibre for the given CMOS Inverter
25	Design and Simulation of CMOS NAND gate with Design Architect
26	Layout Design using IC station for the given CMOS NAND gate
27	Physical Verification using Calibre for the given CMOS NAND gate
28	Design and Simulation of CMOS NAND gate with Design Architect
29	Layout Design using IC station for the given CMOS NOR gate

30	Physical Verification using Calibre for the given CMOS NOR gate
31	Design and Simulation of CMOS AND gate with Design Architect
32	Layout Design using IC station for the given CMOS AND gate
33	Physical Verification using Calibre for the given CMOS AND gate
34	Design and Simulation of CMOS OR gate with Design Architect
35	Layout Design using IC station for the given CMOS OR gate
36	Physical Verification using Calibre for the given CMOS OR gate
37	Design and Simulation of Differential Amplifiers
38	Design and Simulation of Current Mirrors with given specifications
39	Design and Simulation of DACs with given specifications
40	Layout Design using IC station for the given SPICE netlist

VLSI Design(35hrs)

SEMESTER: 7th

COURSE COVERAGE – Focus areas

This course will enhance the knowledge of the students in the most important aspects of VLSI Design. The course has been structured keeping in view the current development in the field of VLSI Design and its effect on the society. The development of the course tries to keep the student abreast with the changes in the semiconductor industry.

The key modules of the framework are

- Concepts of Digital Design using Verilog
- FPGA Architectures & Design Flow
- Concepts of Analog VLSI Design using SPICE
- Analog Design Flow

COURSE OBJECTIVE

This course will enable the students to

- Identify the various steps in VLSI Design flow
- Understand and Differentiate between ASIC & FPGA Design flow
- Understand the basic concepts and programming styles of Verilog HDL
- Implement a given digital system as an ASIC using Mentor Graphics front end and back end tools.
- Identify the various steps in Analog Design flow
- Understand and Differentiate between Digital & Analog Design flow
- Understand the concepts of MOSFETs and CMOS Design

• Design the schematic of any logic gate using CMOS circuits

PRE-REQUISITES:

The students should have a basic knowledge of

- Digital Electronics Circuits
- Analog Electronics Circuits
- Basics of Electronics

TRAINING MODULES

Sl. No.	Topic
1	Mixed–Signal Design Flow
2	Review of Digital Circuit Design
3	Review of Analogue Circuit Design
4	Design and simulation of a digital circuit using HDL Designer
5	RTL synthesis of the digital circuit using Leonardo Spectrum
6	Design & Simulation of an analog circuit using Design Architect
7	Extracting the SPICE code of a digital circuit
8	Extracting the SPICE code of an analog circuit
9	Combining the SPICE of analog and digital circuit
10	Floor planning& Placement of the mixed-signal circuit
11	Routing the net list of the mixed-signal circuit
12	RC Extraction, Post-RC STA of the mixed-signal circuit
13	Concept of DACs and ADCs
14	Design Libraries
15	Static Timing Analysis & Back Annotation
16	Concepts of DFT (BIST, ATPG, Scan Insertions)

17	DFT assertions, Pre & Post DFT Checks
18	Schematic Design using Design Architect
19	Schematic Simulation using Eldo
20	Design & Simulation of Mixed Mode design block using Eldo&Modelsim
21	Project Work

INDUSTRIAL AUTOMATION

COURSE OBJECTIVE:

- Making participants familiar / work with Drive (Hydraulics & Pneumatics) & Control (Manual / Electrical / Electronics) Technology of Industrial related Applications.
- Making participants to know more on Drive & Control specific to their field & new development trends in these areas related to different industrial segments. Our experts in the field shall impart training & share experience with the group
- The Trainees will find this training ideal for optimum use of equipments.

TEACHING AND LEARNING MEDIA:

- Multimedia presentation
- Sample units and power units
- Cut Sections & Transparent Models
- PC animations
- Circuits Simulation on trainer kit
- Circuits Simulation on Automation Simulation Software

INDUSTRIAL AUTOMATION-I

SEMESTER: 3rd &4th

PART-A: - ELECTRICAL HARDWARE CONTROL

- Brief introduction to Electricity.
- Measuring Instruments Details.
- Concept of NO, NC & their Implementation.
- Theories & Practices with Toggle Switch, Push button switch, Limit switch, Selector Switch.
- Relay and Contactor working principle with practical wiring.
- Timer Application Electrical control circuit.
- Star-Delta circuit designing & practices with the use of Timer.

PART-B: - PLC CONTROL

- Introduction to Programmable Logic Controller.
- History of PLC, PLC Architecture.
- Hardware details of PLC.
- Software details of Indra logic works.
- PLC Languages with Ladder Logic Details.
- Assignments on NO & NC.
- Application of SET, RESET Coil with SR, RS.
- Global variable declaration in PLC.
- Application of Timer & Counter in PLC.
- Introduction to IEC based operators.
- Interfacing of PLC with Electrical hardware Components.

Examination: Both Theory & Practical with Submission of Records.

INDUSTRIAL AUTOMATION –II

SEMESTER: 5th

PART-A: - HYDRAULICS

- Applications of Hydraulics Technology in industrial Automation.
- Advantages & Disadvantages of Hydraulics System.
- Theories & Hands on practices of Various Directional & Pressure control Valves.
- Theories & Hands on practices of Flow control Valves, Various Actuators.
- Detailed discussion on Hydraulics Symbols Simulation Software.

PART-B: PNEUMATICS

- Introduction to Pneumatics Technology.
- Difference between Hydraulics & Pneumatics Control.
- Advantage & Disadvantages of Pneumatics Technology.
- Application of Pneumatics Technology in Automation.
- Types of Directional control valves & their Implementation.
- Theories & Hands on practices on Shuttle valve, Twin pressure valve, Time delay valve.
- Theories & Experiments on Flow control valve.
- Practices of Pneumatic circuits in Simulation Software.

PART-C:-ELECTRO- PNEUMATICS.

- Introduction to Electro-Pneumatics.
- Details of Reed Switch & Sensor (Inductive, Capacitive, Optical Sensor).
- Practices with 3/2 solenoid valve, 5/2 Solenoid valve & 5/3 Solenoid valve.

PART-D:-ELECTRO- HYDRAULICS/PROPORTIONAL HYDRAULICS .

- Introduction to Electro-Hydraulics.
- Design of Electro-Hydraulics circuit with Hardware & software.
- Practices with 4/2 solenoid valve, 4/3 Solenoid valve.
- Practice with proportional hydraulics

Examination: Both Theory & Practical with Submission of Records.

INDUSTRIAL AUTOMATION –III

SEMESTER: 7th

PART-A:-**SENSORICS**

- Introduction to Sensorics
- Principle & operation of Inductive, Capacitive, Photo-electric, Magnetic & Ultrasonic sensor.
- Experiments: - Behavior of Inductive, Capacitive, Magnetic sensor.
- Operating range determination of Ultrasonic & Photo-electric sensor.
- Detection of small objects with the Through-beam & Photo-electric sensor.
- Automatic Forward & Reverse of a stepper motor with use of various sensors.

PART-B: - ROBOTICS

- Introduction to Robotics, Types of Robots and Applications.
- Robot Power Transmission Systems.
- Components of CMS Robot and Robot function in mMS kit.
- Determination of Workspace limitation of Robotic kit.
- CMS instructions and Operation through VCP.
- Information regarding Teach-point and Robot positioning.
- Robotic programming through VCP.
- Simple axis-movement program via VCP 08 panel.
- Movement program with MOVE, Output Set/Reset.
- Movement program with abortion of movement.
- Movement program with rounding of the 90 degree turn.
- Set output & WAIT for an input before movement is continued.

PART-C: - MECHATRONICS

- Introduction to Mechatronics System.
- Application of Pneumatic/Hydraulic System in Mechatronics System.
- Identification of different components in various stations of mMS.
- Advanced PLC programming & PLC interfacing with mMS.
- Practices with PLC Networking & Visualization.
- Practices with mMS kit through manual mode with switch and Auto mode with PLC.

PART-D: - DRIVES (VFD)

- Introduction to Variable Frequency Drive System
- Operation of VFD in Material Transfer Station

Examination: Theory & Report Submission.

For feedback and suggestion please write to trainingfeedback@cvrgi.edu.in